REMARKS

This application has been carefully considered in connection with the Examiner's Action. Reconsideration and allowance are respectfully requested in view of the following.

The specification has been amended to correct minor informalities. In correcting the informalities, no new matter has been added. Claims 1, 6, 7, 10, 15 and 16 have been amended and Claims 8-9 and 17-22 have been canceled without prejudice or disclaimer.

Claims 1–22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,907,586 to Katsuragawa et al. In response, the Applicants respectfully traverse the Examiner's rejection and instead submit that Claims 1-7 and 10-16, as above amended, are neither taught nor suggested by the cited art. Accordingly, the Applicants respectfully request the reconsideration and withdrawal of the rejection of Claims 1-22 and the allowance of Claims 1-7 and 10-16.

The Examiner cites Katsuragawa et al. as "substantially teach[ing] a method and a device for signal decision, a receiver and a channel condition estimating method for a coding communication system." Admitting that Katsuragawa et al. does not explicitly teach that the update logic is configured to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions, the Examiner argues that the teaching, by Katsuragawa et al., of a rate converting circuit renders the differences between the claimed invention and Katsuragawa et al. as being obvious to one of ordinary skill in the art at the time that the invention was made.

The Applicants respectfully disagree. Unlike Katsuragawa et al., Applicants' invention is directed to a processor configured to embody a pipelined superscalar processor core. To serve in this capacity, the processor must implement an instruction execution pipeline which includes multiple pipeline stages which concurrently executes multiple instructions in different pipeline stages. More specifically, an instruction prefetch unit fetches instructions and provides the

fetched instructions to an instruction sequencing unit. When the fetched instructions include two Viterbi instructions, the instruction sequencing unit forwards each instruction to a respective processing unit for execution thereby. Upon generally simultaneous execution of first and second Viterbi instructions, update logic executes the shift operations noted by the Examiner.

The foregoing is quite distinct from the teachings of Katsuragawa et al. In contrast to the process configured for execution of multiple instructions in different stages disclosed and claimed by the Applicants, Katsuragawa et al. appears directed to a processor configured such that a single processing unit is capable of executing instructions at an enhanced bit rate. Thus, while Applicants' invention and Katsuragawa et al. may both teach faster processing rates, the respective implementations of that teaching are quite distinct.

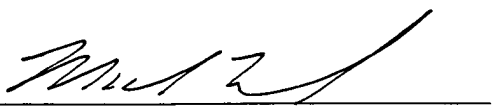
For all the above reasons, the Applicants respectfully request the reconsideration and withdrawal of the rejection of Claims 1-22 and the allowance of Claims 1-7 and 10-16, as above amended.

This application is now considered to be in condition for allowance. A prompt Notice to that effect is, therefore, earnestly solicited.

The Commissioner is hereby authorized to charge payment of any further fees associated with any of the foregoing papers submitted herewith, or to credit any overpayment thereof, to Deposit Account No. 12-2252, LSI Logic Corporation.

Respectfully submitted,
CONLEY ROSE, P.C.

Date: January 30, 2006



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